CLAIMS

[1] A cache memory comprising:

an addition unit operable to add, to each cache entry holding line data, a caching termination attribute indicating whether or not caching of the cache entry is allowed to be terminated;

a selection unit operable to select a cache entry that has been added with a caching termination attribute indicating that caching is allowed to be terminated, and has been set with a dirty flag indicating that the cache entry has been written into; and

a write back unit operable to write back, to a memory, line data of the selected cache entry, regardless of an occurrence of a cache miss.

[2] The cache memory according to Claim 1,

wherein said adding unit includes:

a holding unit operable to hold an address range specified by a processor;

a search unit operable to search for a cache entry holding line data within the address range held in said holding unit; and

a setting unit operable to set, to the searched-out cache entry, the caching termination attribute indicating that caching is allowed to be terminated.

[3] The cache memory according to Claim 2,

wherein said search unit includes:

a first conversion unit operable, in the case where a start address of the address range held in said holding unit indicates a point midway through line data, to convert the start address into a start line address indicating a start line included in the address range;

a second conversion unit operable, in the case where an end address of the address range held in said holding unit indicates a

point midway through line data, to convert the end address into an end line address indicating an end line included in the address range; and

a judgment unit operable to judge whether or not there exist cache entries holding data corresponding to respective line addresses from the start line address to the end line address.

[4] The cache memory according to Claim 2, further comprising

a replacement unit operable, when a cache miss occurs, to select, as a subject for replacement, the cache entry that has been added with the caching termination attribute indicating that caching is allowed to be terminated.

[5] The cache memory according to Claim 1,

wherein said addition unit includes:

an instruction detection unit operable to detect execution, by a processor, of a store instruction having, as instruction details, addition of the caching termination attribute indicating that caching is allowed to be terminated, and writing of data; and

a setting unit operable to set the caching termination attribute to a cache entry that has been written into in accordance with the detected instruction.

[6] The cache memory according to Claim 1,

wherein said write back unit is operable to write back data of a cache entry to the memory, when a memory bus has an idle cycle.

[7] The cache memory according to Claim 1,

wherein each cache entry has a dirty flag for each of a plurality of sub-lines making up one line, and

said write back unit is operable to write back, to the memory, only a dirty sub-line of the cache entry selected by said selection

unit.

[8] A control method for use in a cache memory, comprising:

an addition step of adding, to each cache entry holding line data, a caching termination attribute indicating whether or not caching of the cache entry is allowed to be terminated;

a selection step of selecting a cache entry that has been added with a caching termination attribute indicating that caching is allowed to be terminated, and has been set with a dirty flag indicating that the cache entry has been written into; and

a write back step of writing back, to a memory, line data of the selected cache entry, regardless of an occurrence of a cache miss.